Appendix B
uM-FPU V2 Instruction Timing

The instruction times shown in the following table are calculated from the rising edge of the last byte of an instruction (SIN pin) to the falling edge of the Ready state (SOUT pin). The instruction times do not include the transfer time for sending the instructions to the uM-FPU, which depends on the type of interface (e.g. SPI or I2C), and the speed of the interface.

Transfer time can be minimized by using the 32 byte instruction buffer included in the uM-FPU V2. Instructions can be queued up in the instruction buffer while previous instructions are executing. For a sequence of instructions, the transfer time can overlap the instruction execution time.

There is also a capability for storing user-defined functions in Flash memory on the uM-FPU V2 chip which also eliminates the transfer time.

If debug tracing is enabled, the Ready state is delayed when the trace buffer fills up. Trace data is output through the TSTOUT pin at 57,600 baud. On average, each byte of data in an instruction generates approximately three trace characters, which requires about 521 microseconds to transmit. Once the trace buffer is full, instruction execution is delayed until space is available. When using a fast interface, trace delays can be a dominant part of the overall instruction execution time.

Opcode Name	Data Type	Opcode	Arguments	Returns	Instruction Time (usec)	
SELECTA		0x			35	
SELECTB		1x			35	
FWRITEA	Float	2x	yyyy zzzz		30	
FWRITEB	Float	3x	yyyy zzzz		30	
FREAD	Float	4x		yyyy zzzz	(Note 1)	
FSET/LSET	Either	5x			40	
FADD	Float	6x			120-160	(Note 2)
FSUB	Float	7x			115-170	(Note 2)
FMUL	Float	8x			215-230	(Note 2)
FDIV	Float	9x			330-340	(Note 2)
LADD	Long	Ax			60	(Note 3)
LSUB	Long	Bx			60	(Note 3)
LMUL	Long	Cx			210	(Note 3)
LDIV	Long	Dx			290	(Note 3)
SQRT	Float	E0			1500-1700	(Note 2)
LOG	Float	E1			1800-1850	(Note 2)
LOG10	Float	E2			2000-2050	(Note 2)
EXP	Float	E3			2400-4400	(Note 4)
EXP10	Float	E4			2200-5000	(Note 4)
SIN	Float	E5			2000-2500	(Note 2)
COS	Float	E6			2300-2600	(Note 2)
TAN	Float	E7			4650-5350	(Note 2)
FLOOR	Float	E8			110-155	(Note 2)
CEIL	Float	E9			110-155	(Note 2)
ROUND	Float	EA			155-250	(Note 2)
NEGATE	Float	EB			50	(Note 2)
ABS	Float	EC			50	(Note 2)
INVERSE	Float	ED			330-340	(Note 2)
DEGREES	Float	EE			340	(Note 2)
RADIANS	Float	EF			240	(Note 2)
SYNC		F0		5C	(Note 1)	

FLOAT	Long	F1			95	(Note 3)
FIX	Float	F2			110-140	(Note 2)
FCOMPARE	Float	F3		ss	(Note 1)	
LOADBYTE	Float	F4	bb		100	
LOADUBYTE	Float	F5	bb		100	
LOADWORD	Float	F6	wwww		85	
LOADUWORD	Float	F7	wwww		85	
READSTR		F8		aa … 00	(Note 1)	
ATOF	Float	F9	aa … 00		100-400	(Note 5)
FTOA	Float	FA	ff		1100-3500	(Note 6)
ATOL	Long	FB	aa … 00		40	
LTOA	Long	FC	ff		3100-3250	(Note 6)
FSTATUS	Float	FD		ss	(Note 1)	
XOP		FE			(Note 7)	
NOP		FF			40	
FUNCTION		FE0n FE1n FE2n FE3n			(Note 8)	
IF_FSTATUSA	Float	FE80	ss			
IF_FSTATUSB	Float	FE81	ss			
IF_FCOMPARE	Float	FE82	ss			
IF_LSTATUSA	Long	FE83	ss			
IF_LSTATUSB	Long	FE84	ss			
IF_LCOMPARE	Long	FE85	ss			
IF_LUCOMPARE	Long	FE86	ss			
IF_LTST	Long	FE87	ss			
TABLE	Either	FE88				
POLY	Float	FE89				
READBYTE	Long	FE90		bb	(Note 1)	
READWORD	Long	FE91		wwww	(Note 1)	
READLONG	Long	FE92		yyyy zzzz	(Note 1)	
READFLOAT	Float	FE93		yyyy zzzz	(Note 1)	
LINCA	Long	FE94			35	
LINCB	Long	FE95			35	
LDECA	Long	FE96			35	
LDECB	Long	FE97			35	
LAND	Long	FE98			40	
LOR	Long	FE99			40	
LXOR	Long	FE9A			40	
LNOT	Long	FE9B			40	
LTST	Long	FE9C	ss		(Note 1)	
LSHIFT	Long	FE9D			40-55	
LWRITEA	Long	FEAx	yyyy zzzz		30	
LWRITEB	Long	FEBx	yyyy zzzz		30	
LREAD	Long	FECx		yyyy zzzz	(Note 1)	
LUDIV	Long	FEDx			340	(Note 3)
POWER	Float	FEE0			4300-5700	(Note 2)
ROOT	Float	FEE1			4500-4850	(Note 2)
MIN	Float	FEE2			75	(Note 2)
MAX	Float	FEE3			70	(Note 2)
FRACTION	Float	FEE4			50-60	(Note 2)
ASIN	Float	FEE5				
ACOS	Float	FEE6				
ATAN	Float	FEE7				
ATAN2	Float	FEE8				
LCOMPARE	Long	FEE9		ss	(Note 1)	

LUCOMPARE	Long	FEEA		ss	(Note 1)	
LSTATUS	Long	FEEB		ss	(Note 1)	
LNEGATE	Long	FEEC			35	(Note 3)
LABS	Long	FEED			35	(Note 3)
LEFT		FEEE			35	
RIGHT		FEEF			40	
LOADZERO	Float	FEF0			45	
LOADONE	Float	FEF1			45	
LOADE	Float	FEF2			45	
LOADPI	Float	FEF3			45	
LONGBYTE	Long	FEF4	bb		30	
LONGUBYTE	Long	FEF5	bb		30	
LONGWORD	Long	FEF6	wwww		30	
LONGUWORD	Long	FEF7	wwww		30	
IEEEMODE		FEF8			35	
PICMODE		FEF9			35	
CHECKSUM		FEFA			42000	
BREAK		FEFB			(Note 9)	
TRACEOFF		FEFC			2900	(Note 9)
TRACEON		FEFD			2700	(Note 9)
TRACESTR		FEFE	aa … 00		(Notes 10, 11)	
VERSION		FEFF			80	

Notes:

1. The minimum Read Setup Delay must occur after all opcodes that return data. See the SPI or I^2C instruction timing diagrams for details.
2. The floating point values 1000.0 and 0.001 used for timing.
3. The long integer values 100 and 100000 used for timing.
4. The floating point values 30.0 and 0.001 used for timing.
5. The strings 1.2, 1.23, 1.234, … 1.234567 used for timing.
6. The timing depends on the register value and format specified.
7. The XOP holds Busy state until 2nd byte of an extended opcode is received.
8. The timing depends on the user defined function specified.
9. Busy state is held indefinitely until user continues execution from debugger.
10. Ready state is delayed until the trace buffer is empty.
11. Timing depends on length of trace message.